Current status and Future plans of ALICE FOCAL Project

Taku Gunji
Center for Nuclear Study
University of Tokyo
For the ALICE-FOCAL Team
Outline

• Collaboration
• Summary of physics and measurements
• Requirements of the FOCAL
• Conceptual Detector Design
• Current R&D Status
• Future Plans
• Summary
Collaboration

- Center of Nuclear Study, University of Tokyo, Japan
- Variable Energy Cyclotron Center, Kolkata, India
- Institute for Subatomic Physics and Nikhef, Utrecht University, Netherlands
- Bergen University, Bergen, Norway
- Czech Technical University, Prague, Czech Republic
- ORNL, Oak Ridge, US
- University of São Paolo

- University of Jyväskylä, Finland
- Yonsei University, Seoul, Republic of Korea

More participation from China/Korea are very welcome!!
Physics Motivation of ALICE-FOCAL

• Main physics topics:
  – Gluon saturation (pA)
    • Fully exploit the opportunity at the LHC to access smaller-\(x\) region & large saturation scale by going to forward rapidity.
    • RHIC forward rapidity (\(\eta=3\)) ⇔ LHC mid-rapidity. Importance to understand initial state effects at the LHC (pA).
  – Thermalization mechanism (saturation → glasma) (AA)
  – Systematic measurements of hot and dense medium (AA)
    • Elliptic flow/ridge/jet quenching (AA)
  • Provide forward (\(\eta>3\)) coverage for identified particle measurements
    – EM calorimeters for (prompt) \(\gamma, \pi^0, \eta,\) heavy quark(onia), jets, and correlations (with rapidity gaps)
    – Requires high granularity (lateral and longitudinal)
FOCAL Location and Plans

- **Stage 1** (z=3.5m, 2.5<h<4.5) in 2016
- **Stage 2** (downstream, 4.5<h<6) in 2020
  - Need to modify the beam pipes, flange, valves...

\[ \text{Eta}=2.5 \]
\[ \text{Eta}=3.0 \]
\[ \text{Eta}=4.0 \]
Key Parameters

- **Dynamic range**
  - Annual yield of $\pi^0$ (p+p)
    - $p_T<$30-40GeV is the maximum reach in annual year. $\rightarrow$ 500 GeV in total $E$.

- **Particle density**
  - $N_\gamma \sim N_{ch} \sim 0.03$ /cm$^2$ ($\eta=4$) in p+A
  - $N_\gamma$ is dominated (95%) by low $p_T(<1$GeV) $\gamma$

# of $\gamma$ in FoCAL in central p+Pb (Pb going direction)
Requirement of the FOCAL

• Requirements of the FOCAL
  – High granularity to cope with high multiplicity environment
  – Adequate x and y position resolution, and energy resolution
  – Adequate Level-0 trigger generation
  – Adequate rejection of charged hadrons

• Favored technology: W+Si sampling calorimeter
  – Readout: Si Pad (~1x1cm²)/Si Strip/Si pixel (~0.1x0.1mm²)

<table>
<thead>
<tr>
<th>Readout</th>
<th>Pros</th>
<th>Cons</th>
</tr>
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<tbody>
<tr>
<td>Pad</td>
<td>Good energy resolution, trigger capability</td>
<td>double-hit resolution, occupancy, dynamic range</td>
</tr>
<tr>
<td>Strip</td>
<td>Excellent position resolution, energy resolution</td>
<td>Ambiguities for high multiplicity, occupancy, ghost pairs</td>
</tr>
<tr>
<td>Pixel</td>
<td>Excellent position resolution, High multiplicity</td>
<td>Huge # of channels, smaller bits, slow for readout (usually need L0 trig.)</td>
</tr>
</tbody>
</table>
Conceptual Detector Designs

• Design-I
  – “Standard” W+Si (pad/strip) sampling calorimeter
    • Similar to the PHENIX FOCAL but 3.5m away from IP
    • Pad readout for energy measurement. Pad size ~ Moliere radius
    • Strip in preshower stage for position measurement.

• Design-II
  – W+Si pixel sampling calorimeter
    • Idea from Si pixel detector utilized as tracking device
    • Pixel size ~ 0.05x0.05, 0.1x0.1mm²
    • Monolithic Silicon Sensors [MAPS] (MIMOSA, LePix, SoI, etc)
    • Readout only 1 bit

• Design-III
  – Possible combination of (I)+(II)
    • Pad + pixel (preshower) readout. Pixel size ~ 0.1x0.1, 0.5x0.5, 1x1 mm²
Working Items and Main Players

• Design-I/Design-III
  – Simulation
    • CNS/Prague (features)
    • VECC (clustering)
  – Construction/Mechanics
    • CNS (Si/W/(Mechanics))
    • Prague (Mechanics)
  – ASICs
    • CNS
    • ORNL
  – Digital/DAQ
    • None...
    • Hope to collaborate with EMCal/DCal colleagues.

• Design-II
  – Simulation
    • Utrecht
  – MAPS
    • Strasbourg (MIMOSA)
  – Construction/Mechanics
    • Utrecht
  – DAQ
    • Bergen
**Conceptual Detector Design-I**

- **“Standard” W+Si (pad/strip) calorimeter**
  - W thickness: 3.5 mm (1X₀)
  - wafer size: 9.3cm x 9.3cm x 0.525mm
  - Si pad size: 1.1x1.1cm² (64 ch/wafer)
  - W+Si pad: 21 layers
    - 3 longitudinal segments
    - Summing up raw signal longitudinally in one segment
  - Single sided Si-Strip (2X₀-6X₀)
    - 2γ separation, 6 inch wafer
    - 0.7mm pitch (128ch/wafer)
  - My personal interests to replace strip to pixel (1x1mm² or 0.5x0.5mm²)
Detector Performance (Simulation)

- Detector simulation

Resolution:

\[ 22\% / \sqrt{E} + 1.6\% \]

Position resolution by the strips at 4, 5, and 6 layer.

Resolution \~ 0.25mm with 0.7mm pitch

Linearity <1% up to 200GeV
\[ \pi^0 \] Reconstruction (Simulation)

- **Single \( \pi^0 \) reconstruction**
  - Left: \( \pi^0 \) reconstruction efficiency by pads (inv. mass)
  - Right: \( \pi^0 \) reconstruction efficiency by strips & pads (energy vs. 2 gamma distance)

- **Full simulation (p+p/p+Pb) by T. Tsuji.**

![Graphs showing π^0 reconstruction efficiency](image)

- Efficiency > 50% for E<50 GeV
- Efficiency > 50% for E>60 GeV
Quarkonia Reconstruction
(Simulation)

• Quarkonia simulation
  – Mass resolution: 4% for J/ψ and 3% for Y
  – Full simulation will be done.
Clustering Study (VECC)

- Development of clustering logic (VECC)
  - Data cleanup with a small Edep(ADC) threshold
  - Clustering of showers by newly developed Dynamic FCM (dFCM)
  - 2-3mm separation can be achieved. (π⁰ E>200 GeV)

- Embed 4 gammas with 5mm separation.
- Cluster reconstructed based on the dynamical fuzzy c-mean Method (d-FCM).

**Legend**
- Data count
- Total energy deposition in MeV
**Readout Flow**

- **Composition**
  - **Summing board**: (1.5mm thickness)
    - sum up signals in segments longitudinally, biases
  - **ASIC cards**:
    - Preamplifier + shaper (analog out) or QTC (digital out)
  - **ADC(12-14bit)/TDC(TMC)+FPGA board**:
    - Digitizer, ZS, feature extraction, formatting, trigger handling, buffering
  - **SRU (scalable readout unit)**:
    - Developed by RD51. Trigger handling, data format & transfer, master of slow control
Spec. of our Si pad/strips

- Production of pads/strips by HPK from 6 inch wafer.
  - 25 Si pads and X strips are in our lab.
  - QA was done by HPK.
- Pads: $C_d=25-30\text{pF}$, $I_d=2-10\text{nA}$

Size: 9.3x9.3 cm²
Thickness: 535μm
Pad size: 1.1x1.1 cm²
Number of pads: 64
ASIC Development

• Pads readout:
  – Dynamic range: 50fc – 200pC. Cross talk < 1%. S/N=10@MIP
  – R&D of the ASIC is being done by CNS+RIKEN/KEK and ORNL
    • Dual charge sensitive preamplifier using capacitive division
    • QTC (charge-to-time converter, no CMOS switches)
    • Dual transimpedance preamplifier

• Strip readout:
  – Dynamic range: 4fc – 2pC.
  – PACE-III (CMS preshower, LHCf W+Si)
    • Discussion to use PACE-III has been started with CMS.

• Pixel readout:
  – R&D of ASIC for pixels (1x1, 0.5x0.5mm²) is under discussion.
Current Status of ASIC R&D

- Two types of prototype ASICs were designed.
  - Dual CSP+shaper with capacitive division and Dual QTC
    - Peaking time: $\tau_{\text{peak}} \sim 2\mu\text{sec}$. Good linearity up to 200pC
    - 1st Prototypes (TMC0.5um) will come to our lab. soon.
    - Plan to develop for faster signal processing.
Future ASIC Developments

- Future ASIC developments
  - Dual transimpedance amplifier
  - QTC without CMOS switches
  - CSP+shaper+(AMC+r-amp/comparator+buffer)+MUX (Pixels)

S. Hayashi’s talk

- High gain (R=1kohm)
- Low gain (R=0.1kohm)
- Saturation avoidance circuit

Input current (0.1pC-150pA)
Output (high, 1kohm) (0.1pC-150pA)
Output (low, 0.1kohm) (0.1pC-150pA)

Under designing
Another Geometrical Idea

- hexagonal towers (ORNL)
  - fit nicely in circles around beam-pipe
  - uses more silicon surface of cylindrical ingot

- triangular pads and ASICs

Detector: \(~40\text{pC}~\) charge out.
Conceptual Detector Design-II

- **W absorber + Monolithic pixel sensor**
  - MIMOSA chips (digital readout) are promising to use.
  - Development has been started.
  - 20um pixel size $\rightarrow$ 100 um pixel size ($10^9$ pixels)
  - suppress data volume, reduce RO time
  - avoid saturation ....
  - GBT/GBR being developed by CERN in the end

- CMOS wafer including thin sensitive volume and electronic layers
- charge from traversing particles collected at diodes
E-Link uses SLVS: Scalable Low Voltage Signaling (Low power / low voltage LVDS)

All GBT chips are part of CERN Project (Gigabit receivers)
MAPS Open Questions and Possible Specs.

- **pixel size:**
  - current designs ≈ 20 µm
  - for FoCal 100 µm?
    - charge collection?

- **data volume:**
  - zero suppression?
  - full frame readout?
  - possible option: GBTX serializer per layer, 4.8 GB/s output via twisted pair

- **power consumption:**
  - currently ≈ 90 mW/cm² sensor
  - ≈ 60 kW total
    - tolerable?

- **readout time:**
  - 40 µs total RO time
    - (200 rows)
  - has to be shortened
    - limit near ~10 us

option worked out
Detector Performance (Simulation)

- Detector simulation for pixels

- Energy projection from all layers in case that two gammas are injected with 5mm separation.
  - good separation capability
  - this is conformed up to 2.5mm at least. Still under studying.
Letter of Intent

A Forward Electromagnetic Calorimeter (FoCal) in the ALICE experiment

The FoCal Collaboration

February 21, 2011

Abstract

We intend to build a Forward Electromagnetic Calorimeter as an upgrade of the ALICE experiment at the CERN LHC. The detector should measure photons in the pseudorapidity range $2.5 < \eta < 4.5$ for energies up to $E \approx 500\text{GeV}/c$. It should allow to discriminate direct photons from neutral pions in a large momentum range and should also provide reasonable jet energy measurements. It is intended to be used in collisions of $p+p$, $p+A$ and $A+A$. In 2015 the detector (phase 1) is envisaged to replace the currently implemented Photon Multiplicity Detector (PMD) at a distance of 3.5 m from the interaction point. It will consist of a silicon-tungsten sandwich calorimeter with a combination of silicon pad and silicon strip readout. The detector will also be helpful in the R&D for another detector of similar technology to be potentially implemented at even larger pseudorapidity in the future (phase 2).

1. Physics Motivation
2. Conceptual design of FOCAL
3. Mechanics
4. Electronics
5. Standalone performance
7. Prototype and test results
8. Detector calibration and Monitoring
9. Time schedule
10. Cost estimation

Participation is very welcome!
Preparation of beamtest

• Requesting FOCAL beamtest at CERN-PS/SPS
  – Possible time slot:
    • H2 beamline (EHN1) in SPS (???) : Not fixed yet.
  – Purposes:
    • Evaluation of detector performances
    • Compatibility to ALICE DAQ system/DATE format
  – Readiness by then:
    • One tower of W+ Si pad calorimeter and corresponding ASICs
      – Plans for further downstreams (TRU/SRS) will be discussed. No main workers have been assigned.
    • Partial of W+ MIMOSA pixel calorimeter
Summary

• Current FOCAL activities are reported.

• 2 major design candidates (and possible combination).
  – Standard “W+Si pad/Si strip in preshower” configuration
    • Simulation study and hardware development are on going.
      – Full simulation in p+p/p+A was done and full simulation in A+A is needed.
      – ASICs and Mechanics are under development.
    • Development of digital parts (ADC/TRU/SRS) has not been started...
  – W+Si pixel configuration using MAPS techniques
    • Simulation study and hardware development are on going.
      – Basic performance is studied and full simulation will be done.
      – Newly developed MIMOSA chip is under construction.

• Letter of Intent is being written.

• Beamtest is planed around Nov. in 2011.

• Any participation is very welcome!! We eagerly need you!
Backup slides
**Pi0 reconstruction using Si-Strips**

- Two clusters in the Si-pads start to merge into one cluster when the two-hit distance is below 2cm (for 1cm x 1cm pads)
- Locate a cluster with large energy deposit in the Si-pads & define search region in the Si-strips
- Search for two clusters & obtain distance between the clusters
ADC/TDC & FPGA board

• At least, 10 bit is not enough. More than 12 bit.
  – Commercial FADC (TI, AD„„,) with multi-channel/chip, 10-50MSPS, low power consumption
  – Roughly speaking, data size in p+A could be:
    • \[0.3\text{(occupancy)} \times 256 \text{(tower)} \times 64 \times 3 \text{(ch/tower)} \times 2 \text{(H/L)} \times 12 \text{(bit)} \times 20 \text{(# of samples)} = 0.9MB/event\]
      – Reference: \(dN/dy=700, 15MB/evt \text{ (TPC), 1.1MB/evt \text{ (TRD)}}\)
    • Need to extrapolate to A+A
  – FPGA (Xilinx Virtex series) for zero suppression, feature extraction (online pulse shape analysis, summation), event building, formatting, trigger input handing, output buffering (and send to SUR)
  – Similar to TRU in PHOS/EMCAL.
**FEE & SRU**

- Use SRU as EMCAL/DCAL/(TPC) will do.
  - developed by RD51+ALICE project

*Scalable readout Unit (SRU)*

*TTCrx interface for trigger handling*

10 GBE, SPF, optical fiber

*Master for the slow control of FEEcards*
**Scheme: FEE and SRU**

**DTC link protocol**

proposed by Fan Zhang, CCNU Wuhan

Coded trigger and Control for dynamic actions.
with 80 MHz clock: Input stream from 40 FEC’s @ 80 Mbit/s ~ 3.2 Gbit/s to DATE

Clock $\leftarrow$ DTC_CLK clock to FEC  \hspace{1cm} pin 1-2  
Data $\rightarrow$ DTC_DATA data from FEC  \hspace{1cm} pin 4-5  
Select $\leftarrow$ DTC_TRIG coded trigger to FEC \hspace{1cm} pin 3-6  
Return $\rightarrow$ DTC_RETURN status or local trigger \hspace{1cm} pin 7-8

4 x twisted pairs CAT6 shielded cable

**Note:** for disabling a FEE card, SRU stops CLK for its link
Preamplifier

- Three different types of readout amplifier:
  - Charge sensitive amplifier (CSA)
    - Pad output current is integrated on the feedback capacitor in CSA. Best in terms of noise...
  - Voltage amplifier
    - Pad output signal is integrated on the pad capacitance (Cd) and the voltage across the capacitor is amplified. Uniformity of Cd is necessary.
  - Current amplifier
    - Pad output signal is directly amplified and transformed into a voltage signal. Low input impedance and this limits the use in systems with large capacitive loads...
**Dual charge sensitive preamplifier**

- **Due to the limited output swing of ASIC (5V, 3.3V, 2.5V depending on process), dual input preamplifier with dual gain is designed.**

- **Requirements:**
  - Open loop gain is sufficiently larger compared to the capacitance \( Z = \frac{1}{\omega C + r/A}, \quad \frac{1}{\omega C} >> r/A \)
  - Input impedance \( Z \) is sufficiently smaller compared to \( C_d \)

CSA in high gain side has additional saturation avoidance circuit to keep the constant input impedance of high side.
Next plans including trigger capability

• Revisit our charge sensitive preamplifier
  – To enlarge bandwidth, phase margin, open (closed) loop gain

• Another type of QTC without CMOS switches and shaper
  – Design is underway.

• Another type of preamplifier
  – Voltage amplifier proposed by Chuck (ORNL)
    • Pad output signal is integrated on the pad capacitance (Cd) and the voltage across the capacitor is amplified.
    • Source follower at the 1st stage
      – See Chuck and David’s slides shown in last week.
  – Current amplifier
    • Pad output signal is directly amplified and transformed into a voltage signal. Low input impedance and this limits the use in systems with large capacitive loads...
**Voltage amplifier**

- Shown by Chuck & David (ORNL) last week
  - Quick simulation using LTSPICE (by Taku)

- Input current (5pC/100MIP)

- Voltage at input gate

- Output V (low side)

- Output V (high side)

- Linearity (high/low)

- Voltage at input gate

- Output V (low side)

- Input current (5pC/100MIP)

- Output V (high side)

- Linearity (high/low)
Current preamplifier

- **LTSPICE simulation (Taku)**

  - **Saturation avoidance circuit**
  - **High gain (R=1kohm)**
  - **Low gain (R=0.1kohm)**

Input current (0.1pC-150pA)  
Output (high, 1kohm)  
(0.1pC-150pA)  
Fast signal processing!

Output (low, 0.1kohm)  
(0.1pC-150pA)  
Fast signal processing!
Linearity

- Linearity
  - \( V = V(\text{out}) - V(\text{baseline}) \)
  - \( Z_{\text{in}} = 10 \text{Ohm} \)
  - No gain optimization
  - Good linearity is seen.
- Need to optimize CMOS parameters (\( g_m, W/L, I \) etc) and gain according to realistic conditions.
  - One of the crucial issues is how large impedance the transmission line has.
    - We are planning to use long line for raw signal driving (10cm).
    - Conductance, capacitance, resistance should be carefully evaluated.
**QTCv2**

- *QTC without CMOS switches (Taku)*
  - *Constant current feedback by sensing the output voltage.*

![Diagram of V-I feedback circuit]

- **Large gm**
  - High side: 1pC – 100pC (source follower +Cf = 1.8pC)
  - Low side: 1pC - 150pC (source follower + Cf=1.8pC)

Inclination is constant

Inclination is constant
**R&D of Dual CSP**

Chip size 1 mm × 2 mm
One channel for H/L.
20mW/ch

Qin (fC)
6 (= 136 keV)
0.12
18

Noise
FWHM~90keV
(S/N=10@MIP)

Linearity : 10000
0.15 MeV – 1.5 GeV

Dual Ch (Run9, 16 and 17)
One layer, split in two halflayers

one halflayer
- 1.5 mm W
- W is good heat conductor 170 W/mK (Al 240 W/mK)
- estimated heat resistance ~1 K/W
- no additional interconnect layer/ mounting board
One layer, split in two halflayers

1 layer = two halflayers mounted face to face
- 3 mm W
- 16 chips, their dead zones overlapping
- 4 flextails sticking out
- total thickness 1.5 + 0.5 + 0.5 + 1.5 mm
  further reduction towards 0.5 mm in total for sensors and cables seems possible,
  requires gluing all layers together

cooking pipes at sides will be inserted after assembly of tower
these sides for cables
tension rods keep stack together (prototype)
Two gamma separation

- Event display
Another choice of design

- Readout individual layers. Amplification, shaping, digitization, serialization are done behind the wafer.
  - Lower noise compared to raw signal driving on summing board and smaller dead space between towers.


CMS preshower
Forward Calorimeter: Silicon – W Calorimetry

X-Y  Si pixel (3 layers)
0.3 mm thickness (x & y layer each)
Pixel size 0.5 mm * 0.5 mm x 6 mm

W thickness = 3.5 mm

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si Pad</td>
<td>Si thickness</td>
<td>0.3 mm</td>
</tr>
<tr>
<td></td>
<td>Si size</td>
<td>1 cm x 1 cm</td>
</tr>
<tr>
<td>W</td>
<td>W thickness</td>
<td>3.5 mm</td>
</tr>
</tbody>
</table>

Only Tungsten (W)

W thickness 3.5 mm
2. MAPS

minitower for beam test

- 4 chips per layer: 2*19.2 mm in X, 2* 19.2 mm in Y
  - estimated $R_M = 14$ mm
- prototype chip PHASE1/MIMOSA23
  - testchip for STAR upgrade
    - in production
    - test electronics developed in Berkeley
  - 640 * 640 pixels 30 um pitch
  - read-out time 0.6 ms
  - no on-board data reduction
- read-out system
  - chips wire bonded to conventional flexes
  - modified version of test board for 100 chips
MAPS prototype read-out
System Architecture

- Virtex6 FPGA Board + Adapter
- 4 Layers of 4 Mimosa sensors for 1 Board
- 4*7 RJ45 Connectors, LVDS Signals
- SIU + TTC Connectors
- 6 sets of electronics needed for one detector tower.
MAPS prototype read-out
Virtex6 FPGA Board

- Two FMC Connectors
  - More than 100 LVDS signals
- Memory for data buffering
  - DDR3 SO-DIMM (512 MB)
- Communications and Networking
  - 10/100/1000 Tri-Speed Ethernet
  - SFP transceiver connector
  - USB Host Port and USB Peripheral Port
  - PCI Express x8 Edge Connector

- Software development environment was setup.
- Hardware tests are going on.
- Readout firmware and software under construction.
• Schematic design finished.
• Beginning to layout soon.

• 4 layers separately configured and read out
• Sensors of the same layer working synchronously with the same configuration.
• LVDS Signals with Buffering
• RJ45 Connectors
• Analog input for system monitoring.
• Configurable SIU and TTC connections
• Spare IOs for single chip test.
Diagram of new scheme

• All for 1 tower fits in a 19”/2U crate.
• First data sparsification in Spartan6.
• Data buffering and transmission with Virtex6.
• More functionality and flexibility, higher density, lower cost.
• Schematics finished, layout in progress, to be finished in 2 weeks.

• Full speed data flow into two Spartans:
  – 640Mbps/MAPS * 24 * 2 ≈ 32Gbps.

Two layers of connection board

Red:Top
Blue:Bottom

19” crate

Shimin Yang
Virtex 6 dev-board

- Petalinux evaluated
  - Commercially available Linux distribution for Virtex 6
- Beginning to cross compile existing code for petalinux
  - Existing command line interface
  - Software for access to registers of the firmware
- PLB bus in Microblaze core used for now, gives small interface issue, but should be solved soon.
- Plan to use AXI bus when there is better PetaLinux support.
- Software side joined by Høgskolen i Vestfold
Energy surface density

- central Pb+Pb
- 350cm from vertex

<table>
<thead>
<tr>
<th>y</th>
<th>dE_{EM}/dA (GeV/cm^2)</th>
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</thead>
<tbody>
<tr>
<td>3.0</td>
<td>\approx 1</td>
</tr>
<tr>
<td>3.5</td>
<td>\approx 4</td>
</tr>
<tr>
<td>4.0</td>
<td>\approx 15</td>
</tr>
</tbody>
</table>